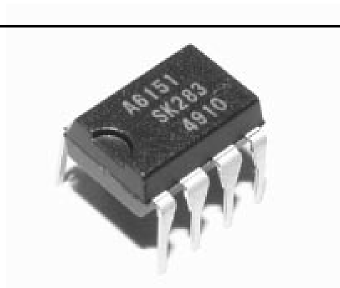
Switching Regulators

PRODUCT DESCRIPTION

Application Note
28103.20



Series STR-A6100
Flyback Switching Regulators

INTRODUCTION

The Series STR-A6100 devices are PRC topology (fixed off-time) designed for relatively low-output power switch-mode power supplies. The controller chips, which adapt Sanken proprietary high-voltage BCD processes, and power MOSFETs, are housed in DIP-8 packages. Therefore, they realize downsizing and reduced cost of power supplies by decreasing external component count and simplifying circuit designs.

The auto-standby function reduces power consumption at light load, while various protections including the avalanche energy guaranteed MOSFET, provide high reliability of system design.

Note: PRC stands for Pulse Ratio Control (on-pulse-width control with fixed off-time).

The off-time of the Series STR-A6100 is fixed at 8 µs.

Features

- Small Size (8-pin DIP) fully-molded package (suitable to low-profile SMPS)
- Built-In avalanche-energy-guaranteed power MOSFET (to simplify surge-absorption circuit; no V_{DSS} derating is required.)
- Built-In Start-Up Circuit (to alleviate power loss by cutting the circuit off after the start-up)
- Burst Stand-By (to realize $P_I \leq 0.1$ W at no load)
- Auto Bias Function (stable burst operation with no affect from transformer)
- Built-In Constant-Voltage Drive Circuit, which is not affected by V_{CC}
- Low Circuit Current in Non-Operation (circuit current before start-up), $I_{CC(OFF)} = 10$ µA
- Low Circuit Current in Operation, $I_{CC(ON)} = 1.5$ mA
- Two Operational Modes by auto-switching functions -
  in normal operation: PRC mode (on-width control with fixed off time)
  in stand-by operation (at light load): burst mode (intermittent operation)
- Built-In Leading-Edge Blanking Function
- Various Protection Functions -
  pulse-by-pulse overcurrent protection (OCP)
  overload protection (OLP) → auto recovery
  overvoltage protection (OVP) → latch mode
  thermal shutdown (TSD) → latch mode

All performance characteristics given are typical values for circuit or system baseline design only and, unless otherwise stated, are at the nominal operating voltage and an ambient temperature of +25°C, unless otherwise stated.

TERMINAL FUNCTIONS

Start-Up (Pin 5)

Figure 1 shows the external start-up circuit. The start-up pin can be directly connected to the rectified high dc voltage. Also, the pin is internally connected to the source of constant current (790 µA). At start-up, the source of constant current charges C2 through the V_{CC} pin and the IC starts its operation when the V_{CC} pin voltage reaches an operation start voltage ($V_{CC(ON)}$ = 17.5 V). After that, the source of constant current will stop its operation and lower its power consumption to a few milliwatts. Start-up time in seconds depends on the source of constant current, obtained by the following formula. For example:

$$t_{start} = C2 \times (V_{CC(ON)} - V_{CC(INT)}) / I_{start}$$
$$= 22 \times 10^{-6} \times 17.5/(790 \times 10^{-6}) = 0.487$$

where C2 = 4.7 to 22 µF, recommended.
A default voltage of C2 is hypothesized as 0 V.

Note: R4 connected to the start-up pin is to prevent malfunction by external noise. 10 kΩ to 47 kΩ is recommended.

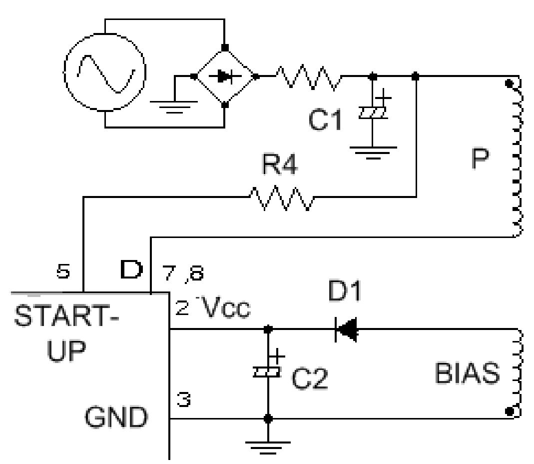


Figure 1 – External Start-Up Circuit

V_{CC} (Pin 2)

Figure 2 shows a relationship between the V_{CC} voltage and the circuit current (I_{CC}). The I_{CC} is low until the control circuit starts its operation ($I_{CC(OFF)}$ = 10 µA at V_{CC} = 15 V, T_A = 25°C), but it goes up rapidly when the V_{CC} pin voltage reaches $V_{CC(ON)}$ = 17.5 V and the IC starts up its operation. After that, the V_{CC} pin voltage falls to $V_{CC(OFF)}$ = 10 V, the IC stops its operation and returns to the initial state.

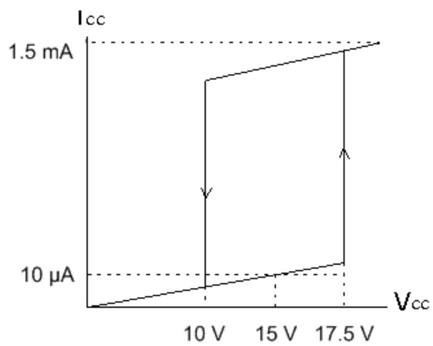


Figure 2 – I_{CC} vs. V_{CC}

Figure 3 shows the behavior of V_{CC} after start-up. As explained, the V_{CC} increases by an internal constant-current source, but it decreases for awhile after the IC starts its operation because the bias winding voltage does not go up enough to charge C2. V_{CC} keeps falling until the bias winding voltage exceeds the falling V_{CC}, then being able to charge C2 and supply power to the IC. Thereafter, V_{CC} is stabilized by the bias winding voltage.

Note: In order to avoid a start-up fault, either the C2 value or the bias winding voltage must be set so that the bottom of the V_{CC} can have a margin, not less than 1 V, against the operation-stop voltage of the $V_{CC(OFF)}$ (10 V).

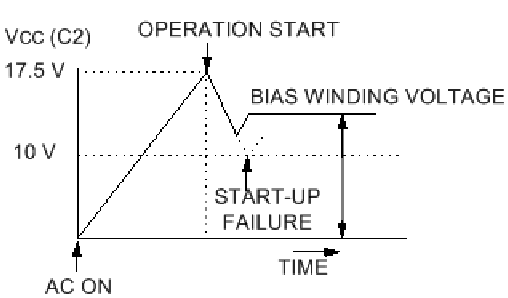


Figure 3 – V_{CC} After Start-Up

■ Bias Winding and R2 (Figure 5): the number of turns in the bias winding should be set so as to become [the $V_{CC(OFF)}$ = 10 V< V_{CC} < $V_{CC(OVP)}$ = 31.2 V]. In general, the bias winding voltage is set between 15 V and 20 V.

As shown in Figure 4, in an actual power supply circuit, the V_{CC} is susceptible to the secondary load. This happens because the primary winding surge voltage is superimposed onto the bias winding, charging the C2 to the peak right after the MOSFET is turned OFF. In order to prevent C2 from charging, as shown in Figure 5, R2 is added. Because a surge voltage is dependent on the structure of the transformer, the winding position of the bias winding also needs to be examined carefully. Furthermore, the optimum value of the resistor should be verified on the bench, which is generally a couple of ohms to

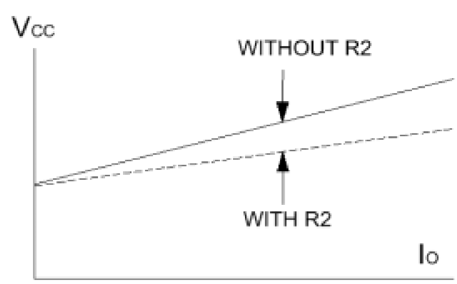


Figure 4 – V_{CC} vs. I_O (Secondary Load)

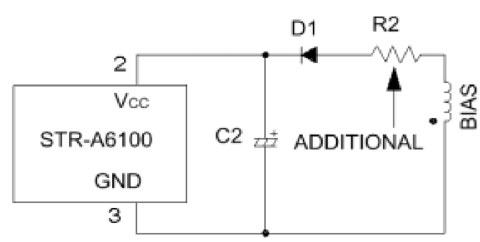


Figure 5 – V_{CC} Peripheral Circuit With R2

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tens of ohms.

OFF Timer and Constant-Voltage Control (FB/OLP, Pin 4)

Figure 6 is a functional block diagram of the STR-A6100 device. Unlike PWM operation, the PRC mode of operation is based on a fixed OFF time (8 µs) and an ON-width (or ON-time) variation. The OFF-timer circuit inside the IC generates the fixed OFF time of the MOSFET and the timing pulse signal for ON starting. The ON period starts right after the end of the fixed OFF period, and terminates when the PRC latch circuit is reset by the ON period termination signal from the OCP or the FB comparator. Thereafter, the OFF timer circuit starts its operation and shifts to OFF period.

Figure 7 shows the operating waveforms for the capacitor voltage inside the OFF timer circuit and for an OCP pin voltage. The OCP pin voltage is detected across R1. The internal capacitor is charged with a fixed slope. If the charged voltage reaches the reference voltage (to negative terminal side) of the comparator, the output (Q\) of the PRC latch turns "Low". Immediately after this happens, the MOSFET turns ON, and at the same time the capacitor is discharged rapidly down to 0 V and keeps the state. In this period, the output MOSFET stays ON, and the drain current I_D runs through the external R1, generating a voltage with the same sawtooth waveform as I_D, the voltage being fed into the OCP pin (Pin 1). This voltage is detected at pin 1, and when the voltage reaches the OCP threshold voltage V_{OCP} = 0.77 V, the OCP comparator resets the PRC latch. Then, the PRC latch output (Q\) turns "HIGH" and the capacitor in the OFF-timer circuit shifts to constant-current charging. From this point of charging to the point of rapid discharge as described above, the fixed OFF time is programmed to be 8 µs. Thus, when the PRC latch output (Q\) is "HIGH", the output MOSFET turns OFF. The above-mentioned ON-period determining operation by the OCP

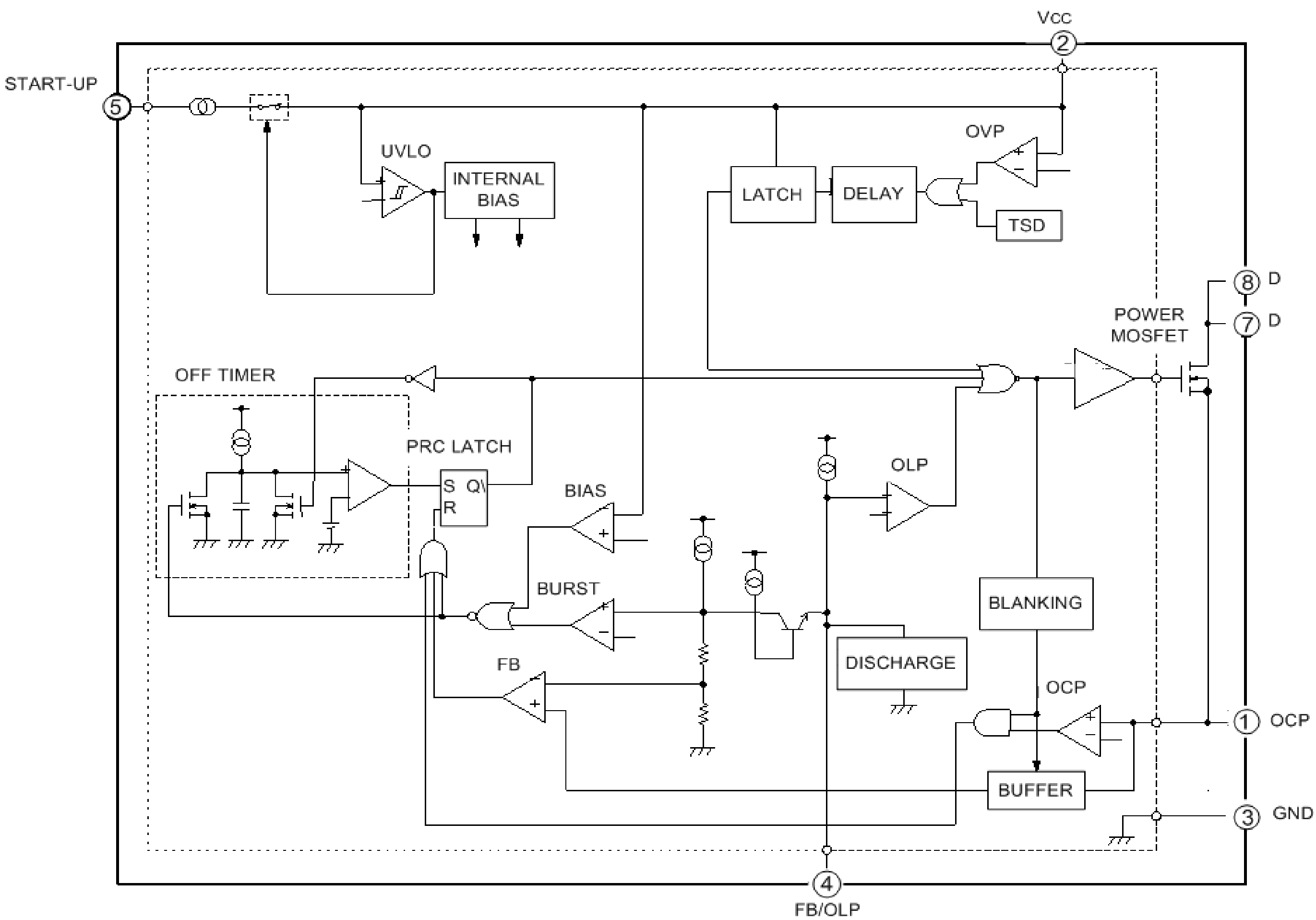

Figure 6 – Functional Block Diagram

comparator works only during start-up. This operation continues until the IC shifts to a constant-voltage control operation mode after start-up. The FB comparator will be explained next because it relates to the ON period, as well.

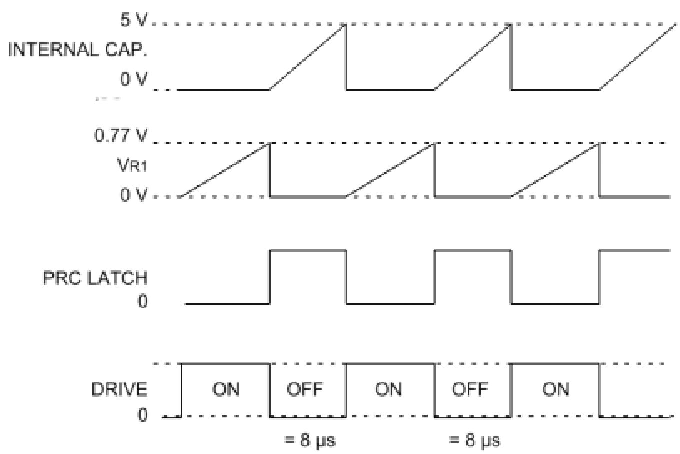

Figure 7 – Internal Waveforms

Figure 8 illustrates a circuit connecting a photocoupler to the FB/OLP pin and explains the feedback operation by the Series STR-A6100 current-mode control. The photocoupler pulls the feedback current (I_{FB}), which is proportional to the signal of the secondary-side error-amplifier (inversely proportional to the secondary-side output voltage), out of the FB/OLP pin. This I_{FB} is obtained through the following procedure: I_{FB} is added to another constant current (I_X), converted to voltage by RFB, and fed into the inverting input of comparator FB as V_{RFB}. Meanwhile, the voltage waveform of R1 (current-sense resistor) is fed into the non-inverting input of FB via the BUFFER block as V_{OCPM}. The FB comparator compares V_{FB1} with V_{OCPM} to reset the PRC latch circuit and to turn off the output MOSFET.

In general, a current-mode control makes phase compensation easy and operational stability excellent. On the other hand, it has a drawback of possible malfunction caused by noises from surge current when the output MOSFET is switched on.

In order to avoid this, the leading spike is blanked out with a time constant of t_b = 320 ns.

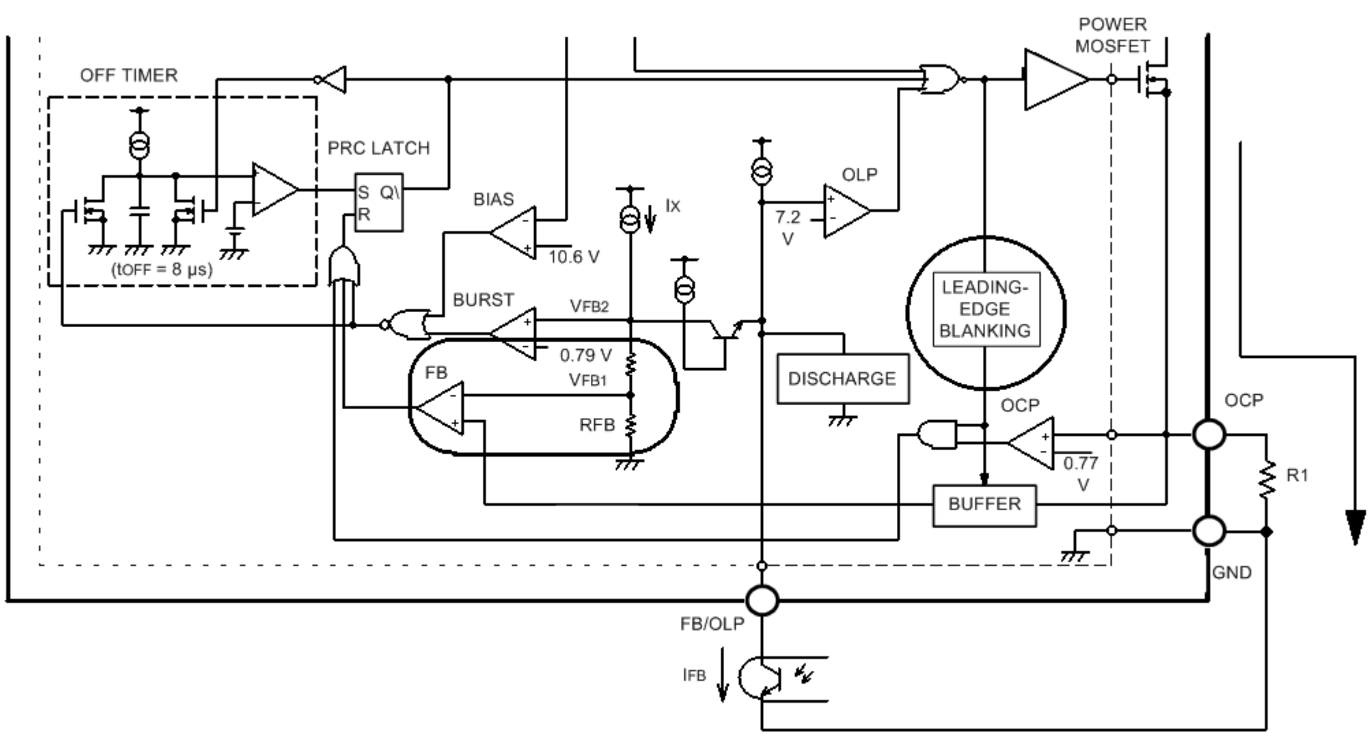

Figure 8 – Current-Mode Control

Overcurrent Protection (OCP, Pin 1)

A pulse-by-pulse circuit configuration, which detects peak drain current in every pulse, is used in an OCP circuit. The maximum output power is determined by the OCP and ac input voltages.

Figure 9 shows the dependence of V_O and I_O upon ac input voltage during an OCP operation (an overload state). The falling slope shows an OCP operation area where V_O decreases as I_O increases, and proportionally, the bias winding voltage decreases. When V_{CC} becomes lower than the operation stop voltage (10 V), the IC stops its operation. After that, the internal constant-current source is turned on again, and V_{CC} increases, reaching the operation-start voltage, the IC is activated again. However, in case the overload state continues, V_{CC} fails to increase, and the IC goes into an operation-stop state again. As long as this overload state continues, the aforementioned chain of operation will be repeated (intermittent operation of UVLO).

When the coupling structure of the transformer is not good between the secondary-side winding and the primary-side bias winding, there are cases where bias winding voltage does not drop and the intermittent operation mode does not begin, even if the output voltage drops at the overload state. Overload protection (OLP) circuitry is incorporated in order to prevent this and to protect the power supply.

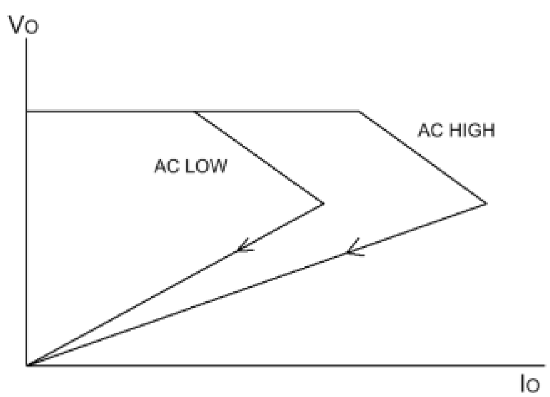

Figure 9 – V_O vs. I_O (Secondary)

Overload Protection (FB/OLP, Pin 4)

The Series STR-A6100 incorporates an overload protection (OLP) circuit. This circuit will stop oscillation when the overload state continues for a certain period (the drain current is limited by the OCP operation).

The peripheral circuit of the OLP is shown in Figure 10. I_{OLP} = 26 µA from the constant-current source is fed into the FB/OLP pin. In the overload state, output voltage at the secondary side drops, and I_{FB} would not be drawn from the error amplifier at the secondary side. Then, C3 is charged by I_{OLP} through the Zener diode. The switching operation is halted until the voltage at C3 goes up to the OLP threshold voltage, V_{OLP} = 7.2 V. After the OLP operation, the aforementioned intermittent operation of the UVLO will be repeated as long as the overload state continues.

■ Voltage Setup of Zener Diode: in normal operation, the voltage at the FB/OLP pin varies within a voltage range determined by I_{OLP} and I_{FB}. Conduction of the Zener diode within this range means that C3 is connected to the optotransistor in parallel. As a result, the load response becomes worse. In general, the recommended value of the Zener diode is 4.7 V to 6.2 V so it cannot be conducted in a normal operation mode.

■ Setup of C3: the value of C3 can be obtained by determining the time from an overload state to an oscillation stop and by getting the delay time, t_d, in seconds from the following:

$$t_d = C3 \times (V_{OLP(MIN)} - V_Z - V_F)/I_{OLP(MAX)}$$

where V_Z = Zener diode voltage and
V_F = Zener diode forward voltage

Notes:
1. t_d should be set to be longer than the start-up time because the start-up mode is considered to be an overload state.
2. Selection of C3 and the Zener diode should be taken into account on the bench.

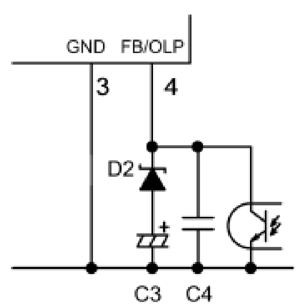

Figure 10 – External OLP Circuit

Auto-Burst Mode (FB/OLP, Pin 4)

Shifting from a normal switching operation to an auto-burst mode is implemented by detecting the voltage at FB/OLP.

Figure 11 shows waveforms at burst mode. At light loads, the I_{FB} of the optotransistor increases, accordingly, the voltage at the FB/OLP pin falls. When the voltage at the FB/OLP pin decreases till V_{burst} = 0.79 V, the internal burst comparator starts its operation and the capacitor in the OFF-timer circuit is shorted to stop the switching operation.

When the switching operation stops, the output voltage at the secondary side slightly decreases. The I_{FB} decreases consequently, and the voltage at the FB/OLP pin rises again up to approximately 1 V. Then, the burst comparator releases the shorted state of the capacitor in the OFF-timer circuit, and a normal switching operation with a fixed OFF time of 8 µs starts. Again, when I_{FB} rises again as the output voltage at secondary side increases, the IC stops switching. Burst mode is a repetition of this chain of operation.

General burst operation at a lower frequency has trouble with audible noise from the transformer. In order to avoid this noise, the IC implements a function that keeps the peak drain current at 25% of that in the normal operation mode.

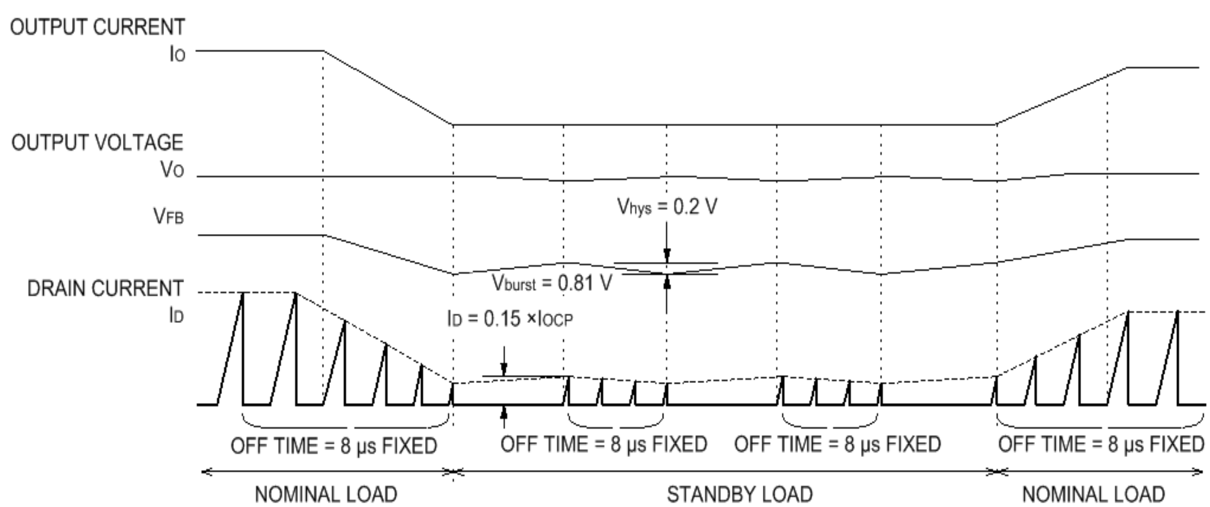

Figure 11 – Burst-Mode Waveforms

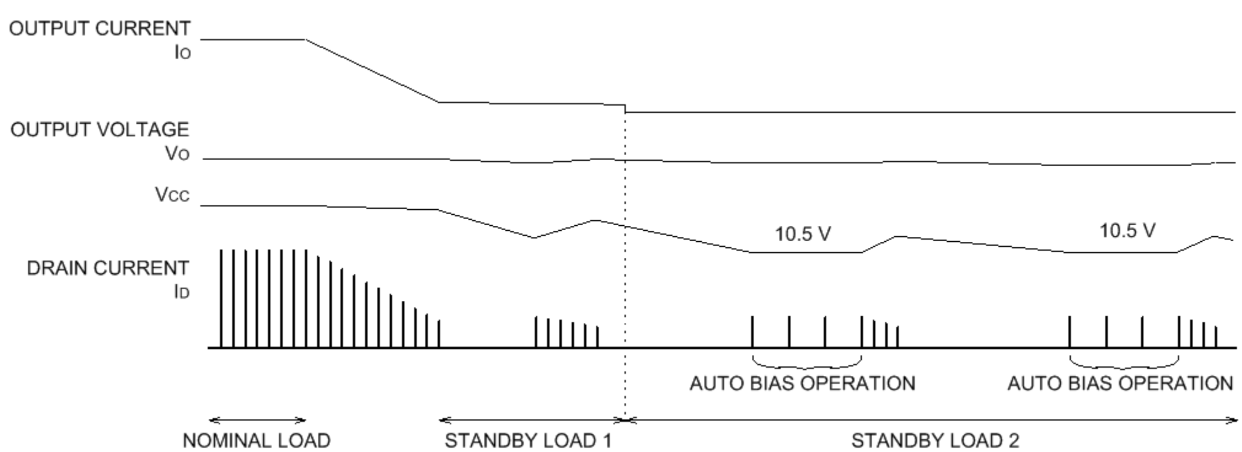

Figure 12 – Auto-Bias Waveforms

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Auto-Bias Function

If coupling between the secondary-side winding and the bias winding is poor from the standpoint of transformer structure, the voltage at V_{CC} might drop at burst mode to the operation-stop voltage, and the IC begins to work in the intermittent operation mode of UVLO.

In order to avoid this, the IC implements auto bias, which forces the IC to work in PRC (Pulse Ratio Control) operation mode when V_{CC} drops to the $V_{CC(bias)}$ = 10.6 V as shown in Figure 12.

A frequent auto-bias implementation results in high power consumption. Thus, it is recommended that the transformer is designed such that V_{CC} does not often drop untill the operation stop voltage.

Latch Circuit

OVP and TSD failure modes are latched by the latch circuit, and the MOSFET is shut down. In order to prevent erroneous mode operation from extraneous noises, a delay time is programmed so that the latch mode can be set only after a certain period of either OVP or TSD operation.

Even in a latched state, the constant-voltage (regulator) circuit is active, circuit current staying at a high level, and the V_{CC} pin voltage decreases. When the V_{CC} pin voltage goes down below the operation-stop voltage, $V_{CC(OFF)}$ = 10 V, the circuit current goes lower than 10 mA (at T_A = 25°C) and the V_{CC} pin voltage rises again by means of the constant-current source. Then, the IC is activated again, the circuit current increasing, and the V_{CC} pin voltage begins to drop. In this way, in a latched mode of operation, the V_{CC} pin voltage goes up and down between 10 V and 17.5 V so it can avoid an abnormal V_{CC} pin voltage rise. Please refer to Figure 13.

The latched mode is released by decreasing V_{CC} to the latch circuit releasing voltage, V_{CC} = 7.3 V. In general, once the ac input is cut off, re-booting is needed.

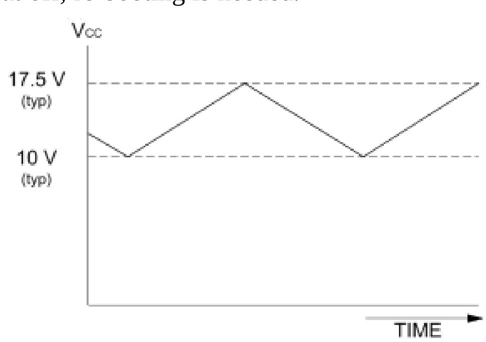

Figure 13 – Latched Mode of Operation

Thermal Shutdown (TSD

Thermal shutdown (TSD) failure mode of operation is latched when the internal frame temperature exceeds 135°C (min).

Overvoltage Protection (OVP)

The overvoltage-protection (OVP) mode of operation is latched when V_{CC} goes up to the $V_{CC(OVP)}$ = 31.2 V. Generally, the V_{CC} pin is connected to the transformer bias winding. Because V_{CC} is proportional to the output voltage, the OVP circuit is effective when the feedback circuit is open and the output voltage rises. The approximate output voltage at OVP operation is obtained from the following formula:

$$V_{O(OVP)} = \frac{V_O \text{ in normal operation}}{V_{CC} \text{ in normal operation}} \times 31.2 \text{ V}$$

CIRCUIT DESIGN CONSIDERATIONS

External Components

- Selecting the optimum value of each external component must depend on an actual load and its variations.
- High-frequency current flows through the current-sense resistor (R1); thus, it is recommended that R1 have a small internal inductance.
- Smoothing capacitors in the primary and secondary side should be high ripple-current types and be intended for switch-mode power supply applications.
- Temperature rise of each component should be allowed for; in particular, the life of the electrolytic capacitor needs to be considered.

Protection Against Negative Input at Start-Up Pin

If there is a possibility that the start-up voltage is more negative than -0.3 V, either a diode or a resistor (33 kΩ) must be added. See Figure 14.

Appropriate diode specifications are:

- Peak reverse voltage (V_{RM}) > 35 V
- Forward current (I_F) > 1.5 mA
- Reverse recovery time (t_{rr}) < 27 µs
- Reverse current (I_R) < 100 µA

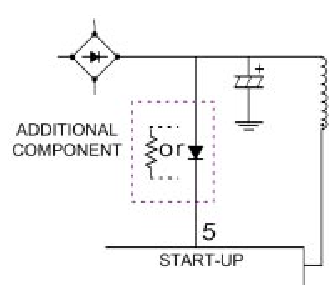

Figure 14 – Added Diode or Resistor

Phase Correction

- Current-mode control topology of the Series STR-A6100 does not require any special phase correction.
- Sanken's error-amplifier ICs (Series SE), which feature phase correction to give consideration to transient response, enable reduction or simplification of the external phase-correction circuit.
- In case of an unstable operation due to unique load requirements or high ripple voltage on the smoothing capacitors, a capacitor (C4 of approximately 680 pF) is inserted as shown in Figure 15.

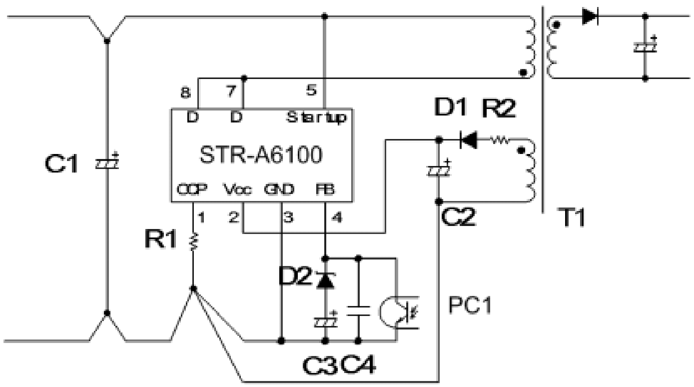

Figure 15 – Typical Connections

LAYOUT CONSIDERATIONS FOR PRC OPERATION

As shown in Figure 15, all traces in the loop from the OCP pin to the drain pins (7 and 8) through R1, C1, and T1, where high current flows, should be kept as thick and short as possible. To eliminate common impedance, the GND pin and its peripheral components should be located as close to R1 as possible.

Component Placement Considerations in SMPS Circuit

As pattern layout and component placement cause malfunction of the device, EMI noise, or power losses in the IC, the following guidelines should be followed:

- Traces where high frequency and high current flow should be kept thick and short to lower line impedance.
- As shown in Figure 16, the hatched area where high frequency and high current create a loop should be kept as small as possible.
- GND and earth lines should be kept as thick and short as possible.
- In SMPS (Switch-Mode Power Supply) circuitry, as traces and paths of high voltage exist, component layout and trace length should be carefully considered, followed by safety requirements.
- Placement of power-supply and heat-sinking designs should be carefully considered on the bench using an actual set.

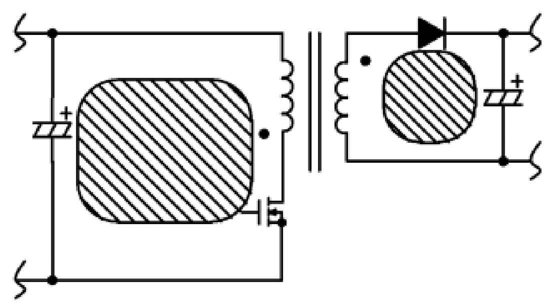

Figure 16 – High-Frequency, High-Current Loops

WARNING — These devices are designed to be operated at lethal voltages and energy levels. Circuit designs that embody these components must conform with applicable safety requirements. Precautions must be taken to prevent accidental contact with power-line potentials. Do not connect grounded test equipment.

The use of an isolation transformer is recommended during circuit development and breadboarding.

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